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FREQUENCY PRESCALER APPARATUS, METHOD, AND SYSTEM

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FREQUENCY PRESCALER APPARATUS, METHOD, AND SYSTEM

Field

The present invention relates generally to frequency divider circuits, and more specifically to digital frequency divider circuits.

Background

Many applications exist for frequency synthesizers. For example, in communications systems, frequency synthesizers can be used to generate local oscillator (LO) signals for modulating and demodulating radio frequency (RF) signals. In these systems, the RF signals can be varied in frequency by varying the frequency of the LO signals.

A frequency synthesizer with a variable output frequency may utilize a feedback loop circuit that includes frequency divider circuits, or "prescalers." A frequency prescaler typically employs a combination of sequential elements and digital logic to provide a variable amount of frequency division. For example, a frequency prescaler may be configured to divide a reference signal by a factor of 4 or by a factor of 5 using flip-flops and digital logic gates. By varying the amount of frequency division provided by the prescaler, the synthesizer output frequency can be varied.

Any given frequency synthesizer has a maximum frequency at which it will reliably operate. This maximum frequency is dependent on many factors, including the topology of the circuit, the underlying manufacturing process, and the maximum operating frequency of the prescaler. If a faster prescaler is available, this may increase the maximum operating frequency of the frequency synthesizer.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternate frequency division mechanisms.

Brief Description of the Drawings

Figure 1 shows a diagram of a prescaler;

Figure 2 shows a circuit schematic of a sequential element;

Figures 3 and 4 show circuit schematics of sequential elements with embedded logic;

Figures 5 and 6 show diagrams of prescalers;

Figure 7 shows a circuit schematic of a sequential element with embedded logic;

Figure 8 shows a diagram of a frequency synthesizer;

Figure 9 shows a system diagram in accordance with various embodiments of the present invention; and

Figure 10 shows a flowchart in accordance with various embodiments of the present invention.

Description of Embodiments

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that the various embodiments of the invention, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein in connection with one embodiment may be implemented within other embodiments without departing from the spirit and scope of the invention. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals refer to the same or similar functionality throughout the several views.

Figure 1 shows a diagram of a prescaler. Prescaler 100 includes flip-flops 102, 104, 106, 108, and 110, inverters 112, 114, 116, and 122, multiplexer 118, and NOR gate 120. Flip-flops 102, 104, and 106 form an asynchronous counter. Flip-flop 102 forms a least significant stage of the asynchronous counter, and flip-flop 106 forms a most significant stage of the asynchronous counter. The counter is referred to as asynchronous because each of the flip-flops in the counter are not clocked by a common clock signal. Rather, each successively more significant stage of the counter is clocked by an output signal from a less significant stage.

Flip-flops 104 and 106 are configured as divide-by-two circuits, in part because the D input is coupled to the inverted output. Flip-flop 102 is also coupled as a divide-by-two circuit, but the divide-by-two action is gated by the second D-input shown as "D2" in Figure 1. Flip-flop 102 is an example of a sequential element having a logic gate embedded within an input stage. An example of flip-flop 102 is shown in more detail in Figure 3.

Flip-flop 110 also includes embedded logic in an input stage. Flip-flop 110 receives four input signals on input nodes shown as D1, D2, D3, and D4, and produces an inverted output. In some embodiments, the embedded logic gate in the input stage of flip-flop 110 may be a four input OR gate. Flip-flop 110 is an example of a decoder flip-flop that uses an embedded logic gate to decode the state of the asynchronous counter and other signals, and gate the input to flip-flop 102. An example of flip-flop 110 is shown in more detail in Figure 4.

In operation, prescaler 100 receives a signal on node 130, and produces an output signal on node 140. Prescaler 100 also receives a signal "M" on node 150 and a signal "P" on node 160. Prescaler 100 divides the frequency of the input signal based on the values of M and P, and produces the output signal having a lower frequency than the input signal.

Prescaler 100 may operate in one of two modes as determined by the state of the M (mode) signal: a 4/5 mode, or an 8/9 mode. When M is set to a logical "1," prescaler 100 operates in the 4/5 mode, and when M is set to a logical "0," prescaler 100 operates in the 8/9 mode. In the 4/5 mode, prescaler 100 divides the frequency

of the input signal by either four or five. In the 8/9 mode, prescaler 100 divides the frequency of the input signal by either eight or nine.

In the 4/5 mode, multiplexer 118 selects the output of inverter 114 to provide the output signal on node 140. Also in 4/5 mode, NOR gate 120 removes the effects of flip-flop 106 from the counter decoding performed by flip-flop 110. In this mode, the state of the "P" signal determines whether prescaler 100 divides by four or divides by five. When P is set to a logical "0," prescaler 100 divides by four, and when P is set to a logical "1," prescaler 100 divides by five.

In the 8/9 mode, multiplexer 118 selects the output of inverter 116 to provide the output signal on node 140. Also in 8/9 mode, NOR gate 120 allows the output of flip-flop 106 to be included in the counter decoding performed by flip-flop 110. In this mode, the state of the "P" signal determines whether prescaler 100 divides by eight or divides by nine. When P is set to a logical "0," prescaler 100 divides by eight, and when P is set to a logical "1," prescaler 100 divides by nine.

Prescaler 100 is an example of an "even/odd" modulus prescaler that can function in one of two even/odd modes: 4/5, and 8/9. The M control signal selects between the different even/odd modes. The P control signal conditionally lengthens the period of the asynchronous counter by one period of the input signal to modify the modulus of the counter between an even and an odd modulus.

In some embodiments, more sequential elements are added to the prescaler to provide even/odd modes other than 4/5 or 8/9. For example, in some embodiments, prescalers provide even/odd modes of 16/17 and 32/33. Any even/odd mode may be provided by a prescaler without departing from the scope of the present invention.

Figure 2 shows a circuit schematic of a sequential element. Sequential element 200 is referred to as a true-single-phase-clock (TSPC) flip-flop, in part because it responds to a single clock signal rather than two clock signals with different phases. Sequential element 200 includes input stage 210 that receives an input signal on a "D" input node and a clock signal on a "CLK" input node. CLK input node 204 is coupled to gates of transistors 212 and 216, and D input node 250

is coupled to the gate of transistor 220. An inverted output is provided at output node 206.

In some embodiments, sequential element 200 is used for one or more of flip-flops 104, 106, and 108 (Figure 1). For example, when sequential element 200 is used for flip-flop 104, CLK input node 204 may be coupled to the output of inverter 112 (Figure 1), and D input node 250 may be coupled to output node 206.

Figures 3 and 4 show circuit schematics of sequential elements with embedded logic. Referring first to Figure 3, sequential element 300 includes input stage 310 that receives input signals on two input nodes: "D1" and "D2." Input stage 310 also receives a clock signal on a "CLK" input node. CLK input node 304 is coupled to gates of transistors 312 and 316, D1 input node 350 is coupled to the gate of transistor 320, and D2 input node 352 is coupled to the gate of transistor 322. An inverted output is provided at output node 306.

Sequential element 300 includes a logic gate embedded in the input stage. For example, transistors 320 and 322 form an OR gate embedded within input stage 310. In some embodiments, sequential element 300 is used for flip-flop 102 (Figure 1). For example, when sequential element 300 is used for flip-flop 102, D1 input node 350 may be coupled to output node 306, D2 input node 352 may be coupled to the output of flip-flop 110, and CLK input node 304 may be coupled to input node 130.

Referring now to Figure 4, sequential element 400 includes input stage 410 that receives input signals on four input nodes: "D1," "D2," "D3," and "D4." Input stage 410 also receives a clock signal on a "CLK" input node. CLK input node 404 is coupled to gates of transistors 412 and 416, D1 input node 450 is coupled to the gate of transistor 420, D2 input node 452 is coupled to the gate of transistor 422, D3 input node 454 is coupled to the gate of transistor 424, and D4 input node 456 is coupled to the gate of transistor 426. An inverted output is provided at output node 406.

Sequential element 400 includes a logic gate embedded in the input stage. For example, transistors 420, 422, 424, and 426 form a four input OR gate

embedded within input stage 410. In some embodiments, sequential element 400 is used for flip-flop 110 (Figure 1). For example, when sequential element 400 is used for flip-flop 110, D1 input node 450 may be coupled to the output of inverter 112, D2 input node 452 may be coupled to the output of flip-flop 104, D3 input node 454 may be coupled to the output of NOR gate 120, D4 input node 456 may be coupled to the output of flip-flop 108, and CLK input node 404 may be coupled to input node 130.

The transistors shown in Figures 2-4 (and later figures) are shown as isolated gate transistors, and specifically as metal oxide semiconductor field effect transistors (MOSFETs). For example, transistors 212, 312, and 412 are shown as P-type MOSFETs, and transistors 216, 316, and 416 are shown as N-type MOSFETs. Other types of switching or amplifying elements may be utilized for the various transistors described herein, without departing from the scope of the present invention. For example, the transistors may be junction field effect transistors (JFETs), bipolar junction transistors (BJTs), or any device capable of performing as described herein.

Figures 5 and 6 show diagrams of prescalers. Referring now to Figure 5, prescaler 500 includes flip-flops 102, 104, 106, 108, and 510, inverters 112, 114, 116, and 122, multiplexer 118, and logic gate 520. As in prescaler 100 (Figure 1) flip-flops 102, 104, and 106 form an asynchronous counter. Flip-flop 102 forms a least significant stage of the asynchronous counter, and flip-flop 106 forms a most significant stage of the asynchronous counter. Flip-flops 104 and 106 are configured as divide-by-two circuits, in part because the D input is coupled to the inverted output. Flip-flop 102 is also coupled as a divide-by-two circuit, but the divide-by-two action is gated by the second D input shown as "D2" in Figure 5. Flip-flop 102 is an example of a sequential element having a logic gate embedded within an input stage. An example of flip-flop 102 is shown in more detail in Figure 3.

Flip-flop 510 also includes embedded logic in an input stage. Flip-flop 510 receives five input signals on input nodes shown as D1, D2, D3, D4, and D5, and

produces an inverted output. In some embodiments, the embedded logic gate in the input stage of flip-flop 510 may be a five input OR gate. Flip-flop 510 is an example of a decoder flip-flop that uses an embedded logic gate to decode the state of the asynchronous counter and other signals, and gate the input to flip-flop 102. In some embodiments, flip-flop 510 may be implemented similar to sequential element 400 (Figure 4) with an additional transistor in parallel with transistors 420, 422, 424, and 426.

In operation, prescaler 500 receives a signal on node 530, and produces an output signal on node 540. Prescaler 500 also receives a signal "M" on node 550 and a signal "P" on node 560. Prescaler 500 divides the frequency of the input signal based on the values of M and P, and produces the output signal having a lower frequency than the input signal.

Prescaler 500 may operate in one of two modes as determined by the state of the M (mode) signal: a 4/5 mode, or an 8/9 mode. When M is set to a logical "1," prescaler 500 operates in the 4/5 mode, and when M is set to a logical "0," prescaler 500 operates in the 8/9 mode. In the 4/5 mode, prescaler 500 divides the frequency of the input signal by either four or five. In the 8/9 mode, prescaler 500 divides the frequency of the input signal by either eight or nine.

In the 4/5 mode, multiplexer 118 selects the output of inverter 114 to provide the output signal on node 140. Also in 4/5 mode, logic gate 520 removes the effects of flip-flop 106 from the counter decoding performed by flip-flop 510. In this mode, the state of the "P" signal determines whether prescaler 500 divides by four or divides by five. When P is set to a logical "0," prescaler 500 divides by four, and when P is set to a logical "1," prescaler 500 divides by five.

In the 8/9 mode, multiplexer 118 selects the output of inverter 116 to provide the output signal on node 540. Also in 8/9 mode, logic gate 520 allows the output of flip-flop 106 to be included in the counter decoding performed by flip-flop 510. In this mode, the state of the "P" signal determines whether prescaler 500 divides by eight or divides by nine. When P is set to a logical "0," prescaler 500 divides by eight, and when P is set to a logical "1," prescaler 500 divides by nine.

Prescaler 500 is an example of an "even/odd" modulus prescaler that can function in one of two even/odd modes: 4/5, and 8/9. The M control signal selects between the different even/odd modes. The P control signal conditionally lengthens the period of the asynchronous counter by one period of the input signal to modify the modulus of the counter between an even and an odd modulus.

In some embodiments, more sequential elements are added to the prescaler to provide even/odd modes other than 4/5 or 8/9. For example, in some embodiments, prescalers provide even/odd modes of 16/17 and 32/33. Any even/odd mode may be provided by a prescaler without departing from the scope of the present invention.

Referring now to Figure 6, prescaler 600 includes flip-flops 602, 104, 106, and 108, inverters 112, 114, 116, and 122, multiplexer 118, and logic gate 620. Flip-flops 602, 104, and 106 form an asynchronous counter. Flip-flop 602 forms a least significant stage of the asynchronous counter, and flip-flop 106 forms a most significant stage of the asynchronous counter. Flip-flops 104 and 106 are configured as divide-by-two circuits, in part because the D input is coupled to the inverted output. Flip-flop 602 is also coupled as a divide-by-two circuit, but the divide-by-two action is gated by other signals received by flip-flop 602. Flip-flop 602 is an example of a sequential element having a logic gate embedded within an input stage. The embedded logic gate decodes the state of the asynchronous counter, receives control signal information, and conditionally allows flip-flop 602 to perform a divide-by-two operation. An example of flip-flop 602 is shown in more detail in Figure 7.

In operation, prescaler 600 receives a signal on node 630, and produces an output signal on node 640. Prescaler 600 also receives a signal "M" on node 650 and a signal "P" on node 660. Prescaler 600 divides the frequency of the input signal based on the values of M and P, and produces the output signal having a lower frequency than the input signal.

Prescaler 600 may operate in one of two modes as determined by the state of the M (mode) signal: a 4/5 mode, or an 8/9 mode. When M is set to a logical "1,"

prescaler 600 operates in the 4/5 mode, and when M is set to a logical "0," prescaler 600 operates in the 8/9 mode. In the 4/5 mode, prescaler 600 divides the frequency of the input signal by either four or five. In the 8/9 mode, prescaler 600 divides the frequency of the input signal by either eight or nine.

In the 4/5 mode, multiplexer 118 selects the output of inverter 114 to provide the output signal on node 640. Also in 4/5 mode, logic gate 620 removes the effects of flip-flop 106 from the counter decoding performed by flip-flop 602. In this mode, the state of the "P" signal determines whether prescaler 600 divides by four or divides by five. When P is set to a logical "0," prescaler 600 divides by four, and when P is set to a logical "1," prescaler 600 divides by five.

In the 8/9 mode, multiplexer 118 selects the output of inverter 116 to provide the output signal on node 640. Also in 8/9 mode, logic gate 620 allows the output of flip-flop 106 to be included in the counter decoding performed by flip-flop 602. In this mode, the state of the "P" signal determines whether prescaler 600 divides by eight or divides by nine. When P is set to a logical "0," prescaler 600 divides by eight, and when P is set to a logical "1," prescaler 600 divides by nine.

Prescaler 600 is an example of an "even/odd" modulus prescaler that can function in one of two even/odd modes: 4/5, and 8/9. The M control signal selects between the different even/odd modes. The P control signal conditionally lengthens the period of the asynchronous counter by one period of the input signal to modify the modulus of the counter between an even and an odd modulus.

In some embodiments, more sequential elements are added to the prescaler to provide even/odd modes other than 4/5 or 8/9. For example, in some embodiments, prescalers provide even/odd modes of 16/17 and 32/33. Any even/odd mode may be provided by a prescaler without departing from the scope of the present invention.

Figure 7 shows a circuit schematic of a sequential element with embedded logic. Sequential element 700 includes input stage 710 that receives input signals on four input nodes: "D1," "D2," "D3," and "D4." Input stage 710 also receives a clock signal on a "CLK" input node. CLK input node 704 is coupled to gates of

transistors 712 and 716, D1 input node 750 is coupled to the gate of transistor 720, D2 input node 752 is coupled to the gate of transistor 722, D3 input node 754 is coupled to the gate of transistor 724, and D4 input node 756 is coupled to the gate of transistor 726. An inverted output is provided at output node 706.

Sequential element 700 includes a logic gate embedded in the input stage. For example, transistors 720, 722, 724, and 726 form a combination OR-AND gate embedded within input stage 710. In some embodiments, sequential element 700 is used for flip-flop 602 (Figure 6). For example, when sequential element 700 is used for flip-flop 602, D1 input node 750 may be coupled to output node 706, D2 input node 752 may be coupled to the output of flip-flop 104, D3 input node 754 may be coupled to the output of logic gate 620, D4 input node 756 may be coupled to the output of flip-flop 108, and CLK input node 704 may be coupled to input node 630.

Figure 8 shows a diagram of a frequency synthesizer. Frequency synthesizer 800 includes voltage controlled oscillator (VCO) 820, frequency prescaler 830, and compare circuit 810. In operation, compare circuit 810 receives a reference signal on node 802, and an output signal from frequency prescaler 830. Compare circuit 810 may compare phases of the two signals or frequency of the two signals and produce a VCO control signal on node 812. VCO 820 receives the control signal on node 812, and produces an output signal on node 804.

VCO 820 may produce an output signal that is greater in frequency than the reference signal on node 802 in part because prescaler 830 divides the frequency of the output signal on node 804. Prescaler 830 may be any of the prescaler embodiments described above. For example, prescaler 830 may be prescaler 100 (Figure 1), prescaler 500 (Figure 5), or prescaler 600 (Figure 6).

Figure 9 shows a system diagram in accordance with various embodiments of the present invention. System 900 includes frequency synthesizer 920, direct conversion receiver 910, and antenna 930. Frequency synthesizer 920 may include any of the even/odd modulus frequency prescalers described above. Further, frequency synthesizer 920 may be implemented using a circuit topology similar to that shown in Figure 8.

Frequency synthesizer 920 may provide a local oscillator signal on node 922, and direct conversion receiver 910 may receive a local oscillator signal at oscillator input port 912. Direct conversion receiver 910 also may receive a signal from antenna 930. Direct conversion receiver 910 may utilize the local oscillator signal to "down-convert" the signal received from antenna 930 directly to baseband. Because direct conversion receiver 910 does not utilize an intermediate frequency (IF), it may also be referred to as a "zero-IF" receiver.

In some embodiments, system 900 includes a transceiver that both transmits and receives signals at antenna 930. For example, system 900 may be a cell phone with a transmitter and a receiver. Also for example, system 900 may be a wireless local area network interface that includes both a transmitter and a receiver. In some embodiments, antenna 930 may be a directional antenna, and in other embodiments, antenna 930 may be an omni-directional antenna.

Frequency synthesizers (and prescalers) may be used in systems other than systems represented by Figure 9. For example, a frequency synthesizer may be used in a system that includes a heterodyne receiver that utilizes an intermediate frequency. Many other system uses exist for frequency synthesizers and prescalers.

Sequential elements, frequency prescalers, frequency synthesizers, and other embodiments of the present invention can be implemented in many ways. In some embodiments, they are implemented in integrated circuits as part of electronic systems. In some embodiments, design descriptions of the various embodiments of the present invention are included in libraries that enable designers to include them in custom or semi-custom designs. For example, any of the disclosed embodiments can be implemented in a synthesizable hardware design language, such as VHDL or Verilog, and distributed to designers for inclusion in standard cell designs, gate arrays, or the like. Likewise, any embodiment of the present invention can also be represented as a hard macro targeted to a specific manufacturing process. For example, frequency synthesizer 800 (Figure 8) can be represented as polygons assigned to layers of an integrated circuit.

Figure 10 shows a flowchart in accordance with various embodiments of the present invention. In some embodiments, method 1000, or portions thereof, is performed by a frequency prescaler, embodiments of which are shown in previous figures. In other embodiments, method 1000 is performed by a frequency synthesizer, an integrated circuit, or an electronic system. Method 1000 is not limited by the particular type of apparatus performing the method. The various actions in method 1000 may be performed in the order presented, or may be performed in a different order. Further, in some embodiments, some actions listed in Figure 10 are omitted from method 1000.

Method 1000 is shown beginning with block 1010 in which a first sequential element is clocked with a voltage controlled oscillator output signal, wherein the first sequential element comprises a true single phase clock flip-flop. In some embodiments, the sequential element referred to in block 1010 may be a least significant stage of an asynchronous counter in a frequency prescaler. For example, flip-flop 102 (Figures 1, 5) or flip-flop 602 (Figure 6) may be clocked by a voltage controlled oscillator output signal when the frequency prescaler is included in a frequency synthesizer such as frequency synthesizer 800 (Figure 8).

In block 1020, a second sequential element is clocked with an output signal from the first sequential element. In some embodiments, the second sequential element referred to in block 1020 may be a next most significant stage of an asynchronous counter in frequency prescaler. For example, the second sequential element may be flip-flop 104 (Figures, 1, 5, 6).

In block 1030, a state of the first and second sequential elements is decoded. The actions of block 1030 may be provided by a flip-flop with an embedded gate, such as flip-flop 110 (Figure 1), flip-flop 510 (Figure 5), or flip-flop 602 (Figure 6). In block 1040, an input signal to the first sequential element is conditionally gated using a logic gate embedded in an input stage of the true single phase clock flip-flop. For example, flip-flops 102 and 602 each conditionally gate an input using a logic gate embedded in an input stage.

Although the present invention has been described in conjunction with certain embodiments, it is to be understood that modifications and variations may be resorted to without departing from the spirit and scope of the invention as those skilled in the art readily understand. Such modifications and variations are considered to be within the scope of the invention and the appended claims.